

FSA2156 — Low-Voltage SPST 0.4Ω Analog Switch

Features




- Maximum 0.7Ω On Resistance (R_{ON}) for +2.7V Supply
- 0.25Ω Maximum R_{ON} Flatness for +2.7V Supply
- Space-Saving MicroPak™ and SC70 Packaging
- Broad V_{CC} Operating Range: 1.65 to 4.3V
- Fast Turn-on and Turn-off Times
- Over-Voltage Tolerant TTL-Compatible Control Input
- Suitable for 2 UL USB2.0 Applications (200mA)
- Low I_{CCT} Current Over Expanded Control Input Range

Description

The FSA2156 is a high-performance Single-Pole Single-Throw (SPST) analog switch that features ultra low R_{ON} of 0.4Ω (typ.) at 2.7V V_{CC} . The FSA2156 operates over the wide V_{CC} range of 1.65V to 4.3V and is fabricated with sub-micron CMOS technology to achieve fast switching speeds. The select input is TTL-level compatible.

FSA2156 features very low quiescent current even when the control voltage is lower than the V_{CC} supply. This feature facilitates longer battery life in mobile handset applications and allows for the direct interface with baseband-processor, general-purpose I/Os.

Ordering Information

Part Number	Top Mark	Pb-Free	Package Description	Packing Method
FSA2156P6	2156		6-lead SC70, EIAJ SC88, 1.25mm Wide	250 Units on Tape and Reel
FSA2156P6X	2156		6-lead SC70, EIAJ SC88, 1.25mm Wide	3000 Units on Tape and Reel
FSA2156L6X	FY		6-lead MicroPak™, 1.0mm Wide	5000 Units on Tape and Reel

Pb-free package per JEDEC J-STD-020B.

Analog Symbol

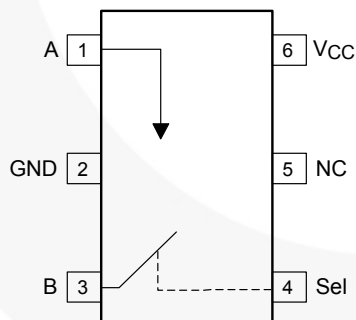


Figure 1. SC70 Pin Assignments (Top View)

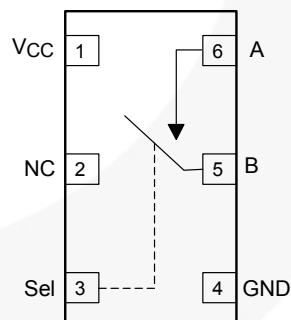


Figure 2. MicroPak™ Pin Assignments (Top View)

Truth Table	
Control Input (S)	Function
L (LOW Logic Level)	Switch Open (OFF)
H (HIGH Logic Level)	Switch Closed (ON)

Pin Descriptions	
Name	Function
A, B	Switch I/O Data Ports
Sel	Control Input

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	4.6	V
V_{SW}	Switch I/O Voltage ⁽¹⁾	-0.5	$V_{CC} + 0.3$	V
V_{CNTRL}	Control Input Voltage ⁽¹⁾	-0.5	4.6	V
I_{IK}	Input Clamp Diode Current	± 50	± 50	mA
I_{SW}	Switch I/O Current (Continuous)		500	mA
I_{SWPEAK}	Pulsed at 1ms Duration, <10% Duty Cycle		500	mA
P_D	Power Dissipation at 85°C	SC70 Package	180	mW
		MicroPak™ Package	180	mW
T_{STG}	Storage Temperature Range	-65	+150	°C
T_J	Maximum Junction Temperature		+150	°C
T_L	Lead Temperature (Soldering, 10 seconds)		+260	°C
ESD	Human Body Model	All Pins	2	kV
		I/O to GND	8	kV
		Charge Discharge Model	2	kV

Note:

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.65	4.3	V
V_{CNTRL}	Control Input Voltage ⁽²⁾	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	0	V_{CC}	V
I_{SW}	Switch I/O Load Current		350	mA
T_A	Operating Temperature	-40	85	°C
θ_{JA}	Thermal Resistance (free air)	SC70 6L package	350	°C/W
		MicroPak™ 6L package	310	°C/W

Note:

2. Control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C			T _A = -40 to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V _{IH}	Input Voltage High		3.6 - 4.3				1.4		V
			2.7 - 3.6				1.3		
			2.3 - 2.7				1.1		
			1.65 - 1.95				0.9		
V _{IL}	Input Voltage Low		3.6 - 4.3					0.7	V
			2.7 - 3.6					0.5	
			2.3 - 2.7					0.4	V
			1.65 - 1.95					0.4	
I _{IN}	Control Input Leakage	V _{CNTRL} = 0 to V _{CC}	1.65 - 4.3				-0.5	0.5	μA
I _{NO(OFF)}	Off Leakage Current of Port B	V _A = 0.3V, V _{CC} - 0.3V, V _B = 0.3V, V _{CC} - 0.3V or Floating Figure 4	1.95 - 4.3	-10		10	-50	50	nA
I _{A(ON)}	On Leakage Current of Port A	V _A = 0.3V, V _{CC} - 0.3V, V _B = Floating Figure 5	1.95 - 4.3	-20		20	-100	100	nA
I _{OFF}	Power Off Leakage Current	Port A V _A = 0.3V, 4.3V, V _{CC} = 0V, V _B = 0V	0V					±25	μA
	Power Off Leakage Current ⁽³⁾	Port A V _A = 0.3V, 4.3V, V _{CC} = 0V, V _B = Floating	0V	-4		+4	-35	35	nA
R _{ON}	Switch On Resistance ⁽⁴⁾ Figure 3	I _{ON} = 100mA, V _B = 0V, 0.7V, 3.6V and 4.3V	4.3		0.36			0.60	Ω
		I _{ON} = 100mA, V _B = 0V, 0.7V, 2.0V and 2.7V	2.7		0.4		0.7		
		I _{ON} = 100mA, V _B = 0V, 0.7V, 1.6V and 2.3V	2.3		0.55		0.80		
		I _{ON} = 100mA, V _B = 0.7V	1.65		1.5				
R _{FLAT(ON)}	On Resistance Flatness ⁽⁵⁾ Figure 3	I _{ON} = 100mA, V _B = 0V, 0.7V, 3.6V and 4.3V	4.3					0.25	Ω
		I _{ON} = 100mA, V _B = 0V, 0.7V, 2.0V and 2.7V	2.7				0.25		
		I _{ON} = 100mA, B = 0V, 0.7V, 1.6V and 2.3V	2.3				0.3		
		I _{ON} = 100mA, V _B = 0V, 0.7V, 0.9V and 1.65V	1.65		0.9				
I _{CC}	Quiescent Supply Current	V _{SW} = 0 or V _{CC} , I _{OUT} = 0	4.3	-100	30	100	-500	500	nA
I _{CCT}	Increase in I _{CC} per Input	V _{CNTRL} = 2.6V	4.3		3			6.0	μA
		V _{CNTRL} = 1.8V			7	12		15.0	

Notes:

3. Guaranteed by characterization; not production tested.
4. On resistance is determined by the voltage drop between A and B pins at the indicated current through the switch.
5. Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.

AC Electrical Characteristics

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t _{ON}	Turn-On Time	V _B = 1.5V, R _L = 50Ω, C _L = 35pF	3.6 - 4.3			55		60	ns	Figure 6 Figure 7
			2.7 - 3.6			60		65		
			2.3 - 2.7			65		70		
			1.65 - 1.95		40					
t _{OFF}	Turn-Off Time	V _B = 1.5V, R _L = 50Ω, C _L = 35pF	3.6 - 4.3			65		70	ns	Figure 6 Figure 7
			2.7 - 3.6			70		75		
			2.3 - 2.7			75		80		
			1.65 - 1.95		90					
Q	Charge Injection	C _L = 1.0nF, V _S = 0V, R _S = 0Ω	2.3 - 4.3		6			pC	Figure 10	
			1.65 - 1.95		1.3					
OIRR	Off Isolation	f = 100kHz R _T = 50Ω	1.65 - 4.3		-65			dB	Figure 9	
BW	-3db Bandwidth	R _T = 50Ω C _L = 0pF	1.65 - 4.3		80			MHz	Figure 8	
THD	Total Harmonic Distortion	R _T = 600Ω, V _{SW} = 0.5V _{PP} , f = 20Hz to 20kHz	1.65 - 4.3		.02			%		

Capacitance

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C			Units	Figures
				Min.	Typ.	Max.		
C _{IN}	Control Pin Input Capacitance	f = 1MHz	0		1.5		pF	Figure 11
C _{OFF}	B-Port Off Capacitance	f = 1MHz	4.3		38		pF	Figure 11
C _{ON}	A-Port On Capacitance	f = 1MHz	4.3		115		pF	Figure 12

Test Diagrams

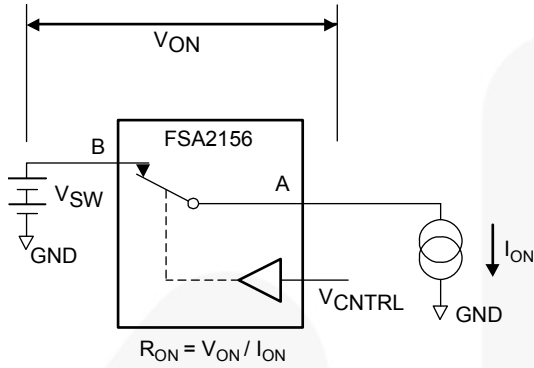


Figure 3. On Resistance

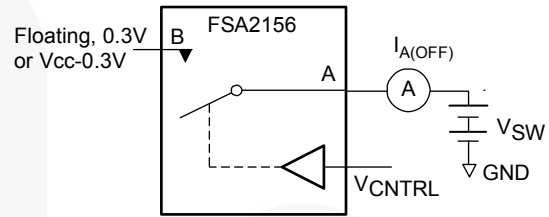


Figure 4. Off Leakage

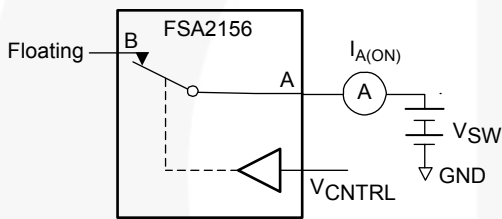


Figure 5. On Leakage

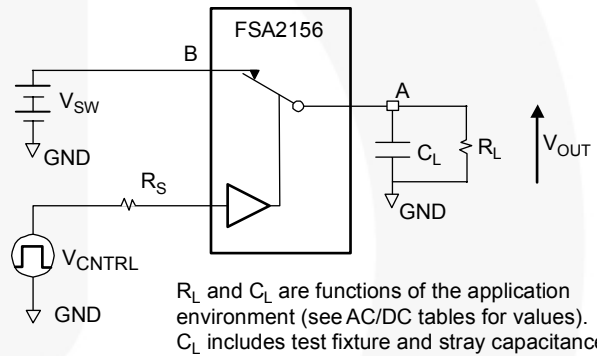


Figure 6. Test Circuit Load

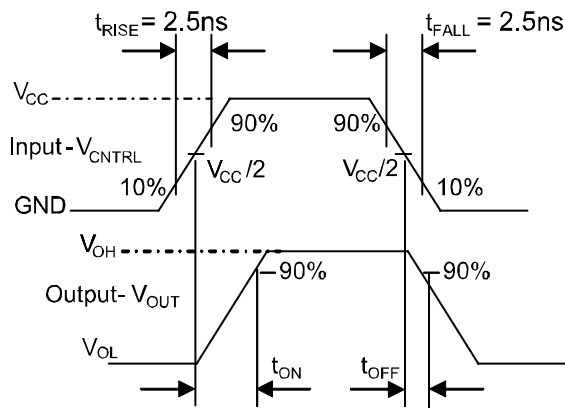
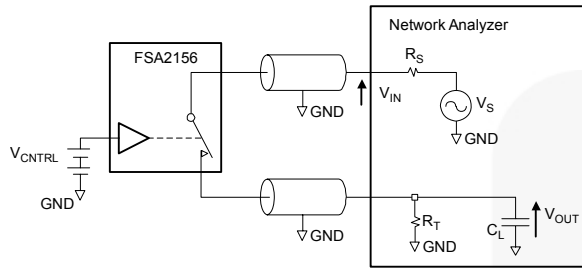


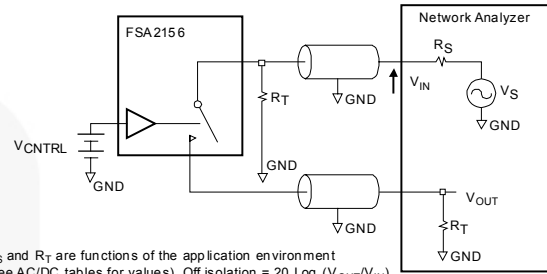
Figure 7. Turn-On / Turn-Off Waveforms

Test Diagrams (Continued)



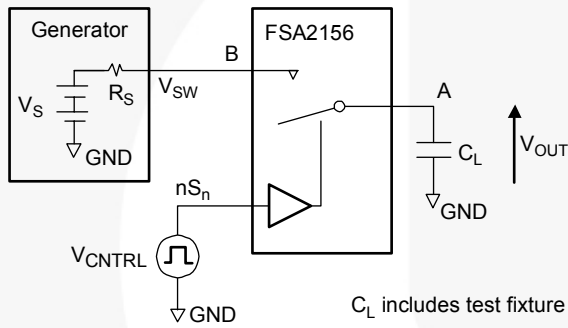
R_T and C_L are functions of the application environment (see AC/DC tables for values). C_L includes test fixtures and stray capacitance.

Figure 8. Bandwidth



R_S and R_T are functions of the application environment (see AC/DC tables for values). Off isolation = $20 \text{ Log } (V_{OUT}/V_{IN})$.

Figure 9. Channel Off Isolation



C_L includes test fixture and stray capacitance

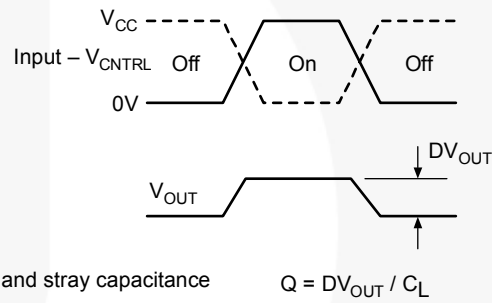


Figure 10. Charge Injection Test

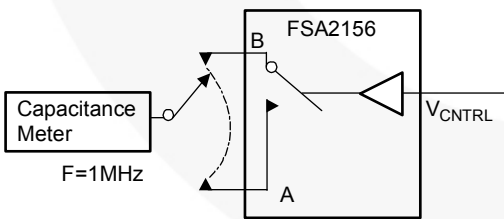


Figure 11. Channel Off Capacitance

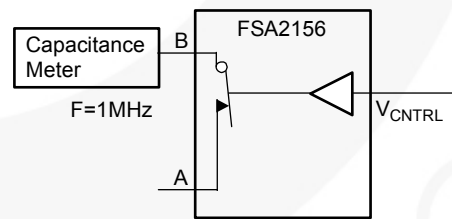
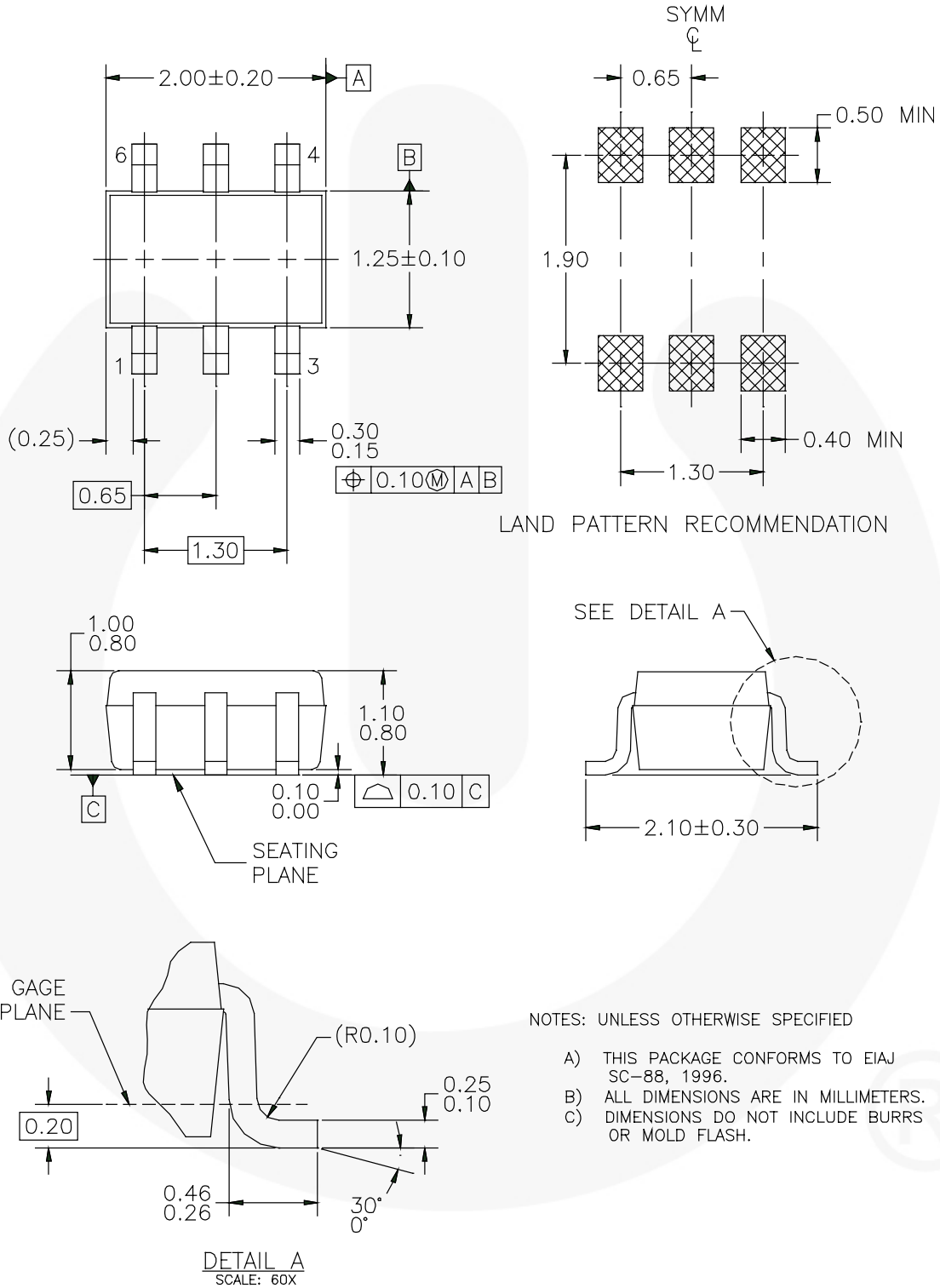


Figure 12. Channel On Capacitance

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



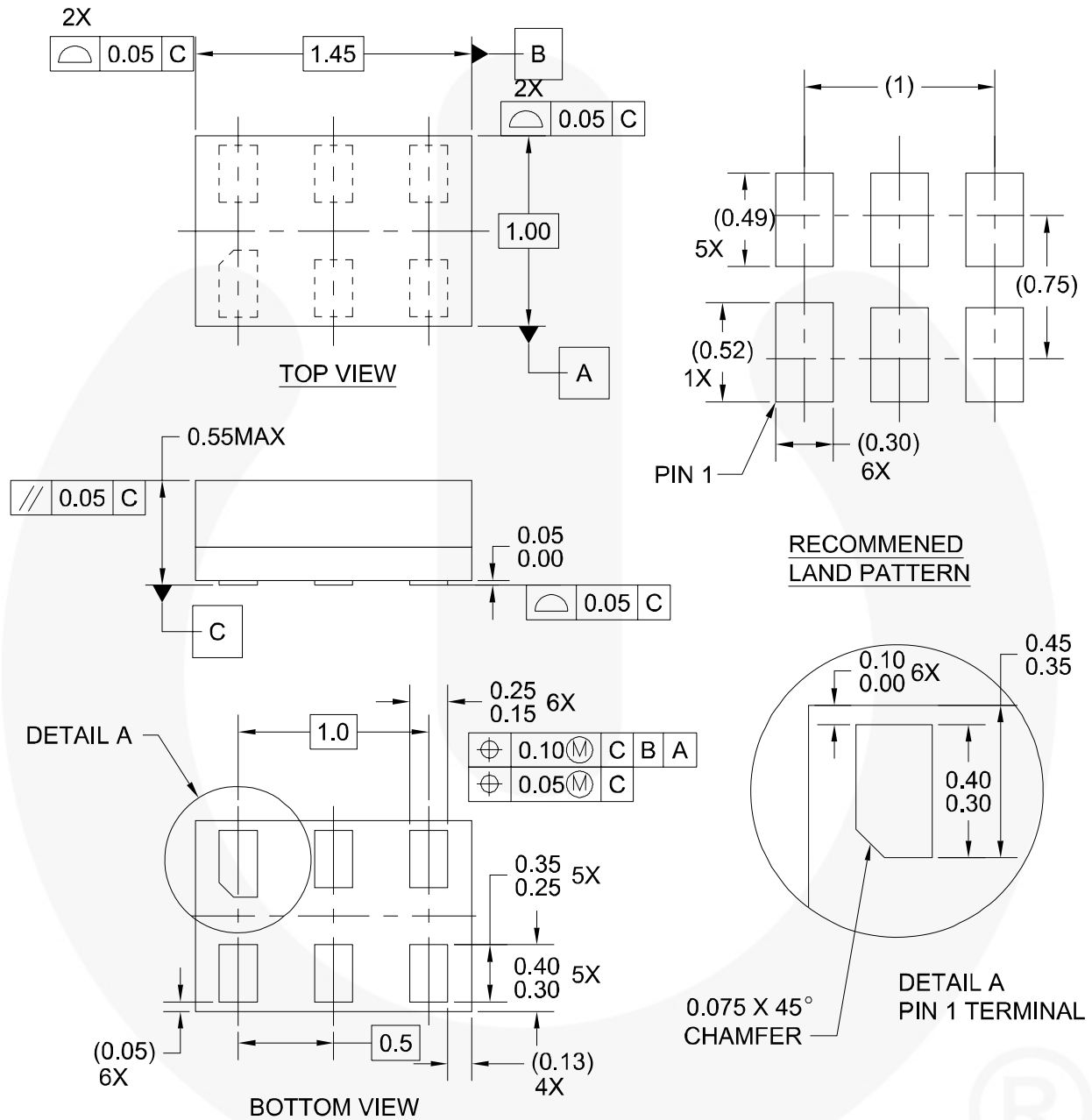
- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO EIAJ SC-88, 1996.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.

MAA06AREV5

Figure 13. 6-Lead, SC70 Package

Physical Dimensions (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.



Notes:

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06AREVC

Figure 14. 6-Lead, MicroPak™ Package

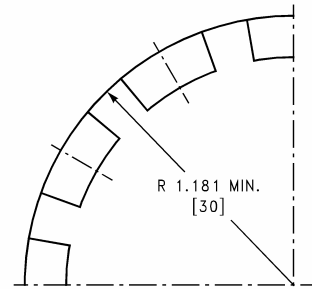
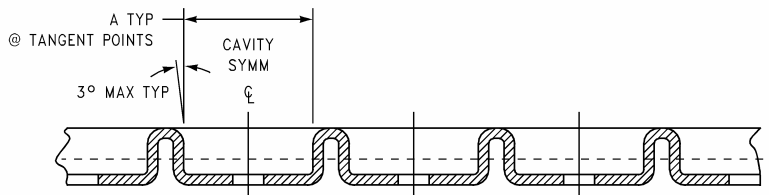
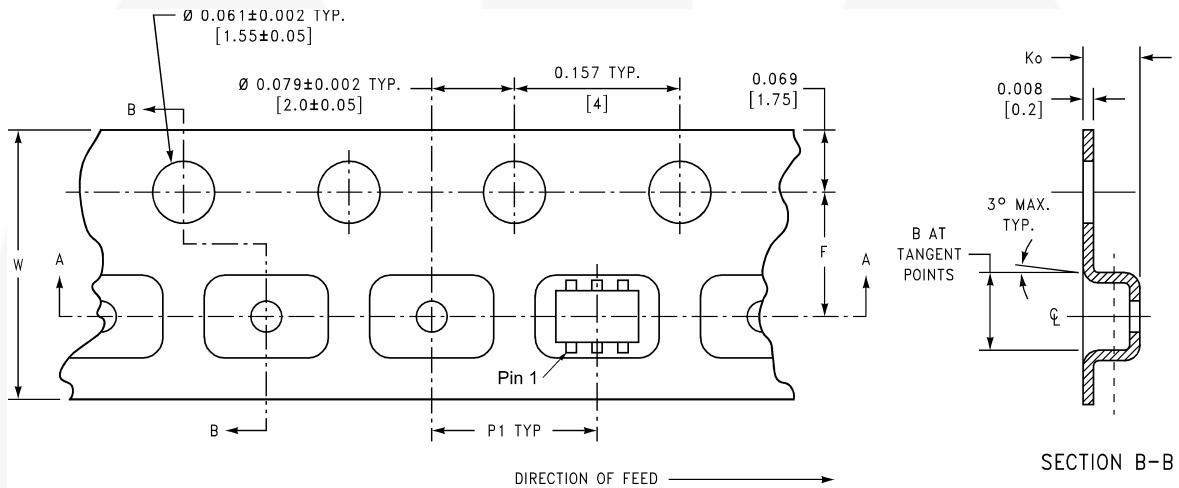
Tape and Reel Specification

Tape Format for SC70

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
P6X	Leader (Start End)	125 (typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typical)	Empty	Sealed

Tape Dimensions

Dimensions are in inches (millimeters).



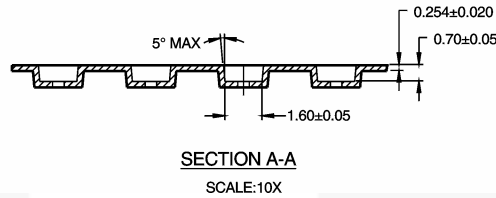
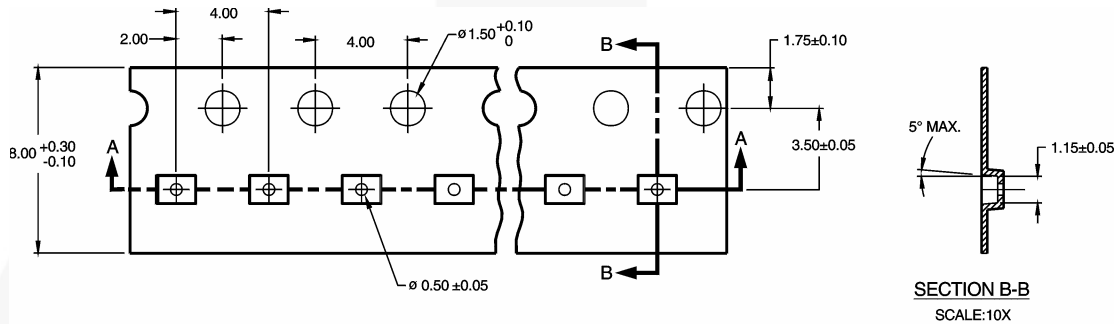
Tape Size	DIM A	DIM B	DIM F	DIM K _o	DIMP1	DIM W
	0.093	0.096	0.138 ± 0.004	0.053 ± 0.004	0.157	0.315 ± 0.004
(8mm)	(2.35)	(2.45)	(3.50 ± 0.10)	(1.35 ± 0.10)	(4.00)	(8.00 ± 0.1)

Tape Format for MicroPak™

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typical)	Empty	Sealed

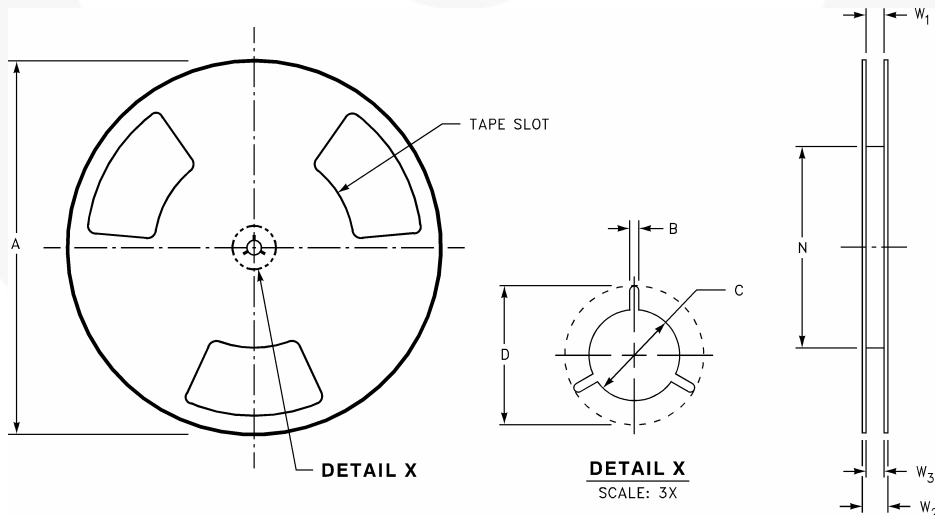
Tape Dimensions

Dimensions are in inches (millimeters).



Reel Dimensions

Dimensions are in inches (millimeters).



Tape Size	A	B	C	D	N	W1	W2	W23
	7.000	0.059	0.512	0.795	2.165	.0331 +0.059 / -0.000	0.567	W1 +0.078 / -0.039
(8mm)	(177.80)	(1.50)	(13.00)	(20.20)	(55.00)	(8.40 +1.50 / -0.00)	(14.40)	(W1 +2.00 / -1.00)



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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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